



Docket No.: 4259P076

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

MARK GREENBERG, ET AL.

Application No.: 09/955,547

Filed: September 17, 2001

For: **An Apparatus and Method For Saturating
Decoder Values**

Art Group: 2133

Examiner: Assignment Division

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Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

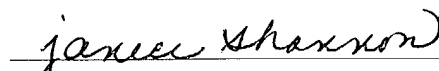


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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet 2 of 3

Complete if Known

Application Number	09/955,547
Filing Date	September 17, 2001
First Named Inventor	Mark Greenberg
Art Unit	2133
Examiner Name	Phung M. Chung
Attorney Docket Number	4259P076

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		HASHIDA MITSUYOSHI, "Hierarchical Network Management System and Control Method For Network Management Information" Patent Abstracts of Japan, Publication No. 07226777	
		MARIE-LAURE BOUCHERET, ET AL, "Fast Convolution Filter Banks For Satellite Payloads With On-Board Processing, IEEE Journal On Selected Areas in Communications, Vol. 17, No. 2, February 1999, pages 238-247.	
		W.H. YIM, ET AL., "On-Board Processing For KA-Band Applications", Publication Date February 11, 1993, University of Surrey, UK, pages 225-229.	
		SUNG HAN CHOI, ET AL., "Viterbi Detector Architecture For High Speed Optical Storage", 1997 IEEE Tencon - Speech and Image Technologies For Computing and Telecommunications, ASIC Center, Corporate Technical Operations SAMSUNG Electronics Co., Ltd., pages 89-92.	
		MICHAEL A. BREE, ET AL., "A Bit-Serial Architecture For A VLSI Viterbi Processor", Communications Systems Research Group, University of Saskatchewan, Saskatoon, IEEE, 1988, pages 72-77.	
		M.A. BREE, ETAL., "A Modular Bit-Serial Architecture For Large Constraint Length Viterbi Decoding", Communication Systems REsearch Group, University of Saskatchewan, Saskatoon, Canada, IEEE, 1990, pages 1501-1506.	
		MARC BIVER, ET AL., " Architectural Design and Realization Of A Single-Chip Viterbi Decoder", Elsevier Science Publishers B.V., Integration, the VLSI journal 8 (1989) October , No. 1, Amsterdam, NL, pages 3-16.	

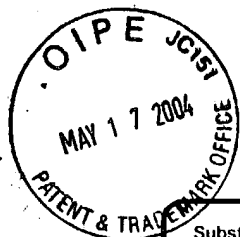
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Sheet

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		JAMES TSUI, "Frequency Channelization, Digital Techniques for Wideband Receivers", Second Edition, Pages 363-396, 2001 Artech House, Inc., Norwood, MA	
		ZHENGDAO WANG and GEORGIOS B.GIANNAKIS, "Wireless Multicarrier Communications where Fourier Meets Shannon", Department of ECE, University of Minnesota, Minneapolis, MN., Pages 1-21.	
		E. VERRIEST, ISEN, Implementing an Adaptive Noise Canceling System to enhance Sonar Receiver Performance Using the TMS320C31 DSP, ESIEE, Paris, September 1996, Texas Instruments, Pages 1-24.	
		GA. SHAW, RA. FORD, J.C. ANDERSON, B.W. ZUERDNORFER, AH. NADERSON, RASSP Benchmard 2 Technical Description, Massachusetts Institute Of Technology Lincoln Library, 153 pages total.	

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